National Aeronautics and Space Administration

FY23 Strategic Initiatives Research and Technology Development (SRTD)

Advanced onboard InSAR processor technology for STV TOs leveraging Xilinx's new Adaptive Compute Acceleration Platform

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Strategic Focus Area: Next Earth Science Decadal Survey: Technology & Architecture for Planetary Boundary Layer (PBL)/ Surface Topography & Vegetation **| Strategic Initiative Leader:** Rashmi Shah

Objectives: To develop advanced algorithms, modeling techniques and libraries to take advantage of new devices that have recently started to come out for space applications, with the goal of implementing a new generation of On-Board Processor (OBP) techniques for Synthetic Aperture Radar (SAR) and for Interferometric SAR (InSAR). Ultimately, the OBP would be packaged to be flown and tested aboard AIRSAR (a long-standing airborne platform operated by JPL, and frequently used for technology experiments).

Background: A new class of space qualified devices are being developed in response to the commercial revolution in space. Of special interest for the world of real-time SAR OBP are the Versal ACAP devices that have been developed and space qualified by AMD/Xilinx. They make available a level of processing that is an order of magnitude greater than that available with the currently used FPGA technology, and the architecture and features should significantly decrease development time.

Approach and Results:The Versal devices combine very large FPGA arrays, System On Chip (SOC) features, and large arrays of specialized processors similar to GPUs (Xilinx refers to these as AI engines), with an architecture designed to support Artificial Intelligence (AI) techniques. We are exploring the trade space of how to partition a real-time radar processing algorithm among the FPGA, SOC, and GPU elements available on the Versal device. This will include the development of modeling techniques and libraries. We are also exploring AI techniques, and how these might be used with SAR OBP.

We have investigated algorithms to be implemented and have settled on and started implementing a back projection algorithm. Back projection is appealing because it is nearly one-size fits all, including airborne, and is well suited to parallelization, but was not practical for implementation in traditional FPGA based real-time SAR processors. Other algorithms more suitable for traditional FPGAs are certainly more efficient, but tend to require careful analysis and tailoring to each case.

Significance/Benefits to JPL and NASA: New devices such as the Versal that are becoming available as a result of the commercial revolution in space, make available an order of magnitude increase in processing power over traditional FPGAs for these applications. But the devices also are much more complex, and require a whole new set of tools and methods to be able to use them effectively, and the learning curve is substantial. To be able to respond effectively to upcoming mission challenges, it is essential that we adopt and learn to use these new devices and methods, and become familiar with the capabilities and limitations of them.

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