FY23 Strategic University Research Partnership (SURP)

Monolithic W-Band Frequency Synthesizer

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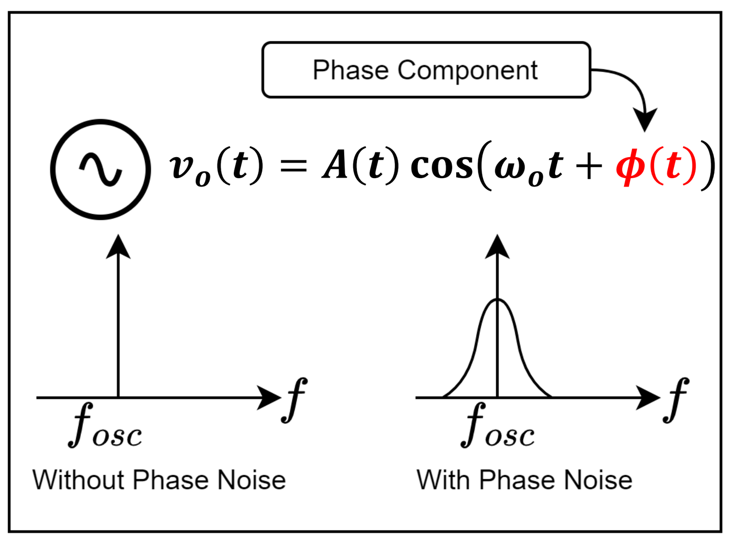
Objectives

Analysis, design, tape-out, and measurements of low-phase-noise millimeter-wave voltage-controlled oscillators in a commercial foundry SiGe HBT process.

Phase Noise



$$\mathcal{L}(\Delta f) = 10\log\left(\frac{k\,T\,F}{2\,Q_L^2\,P_{res}}\left(\frac{f_o}{\Delta f}\right)^2\right)$$

$\mathcal{L}(\Delta f)$: Phase Noise at Δf offset of carrier f_o

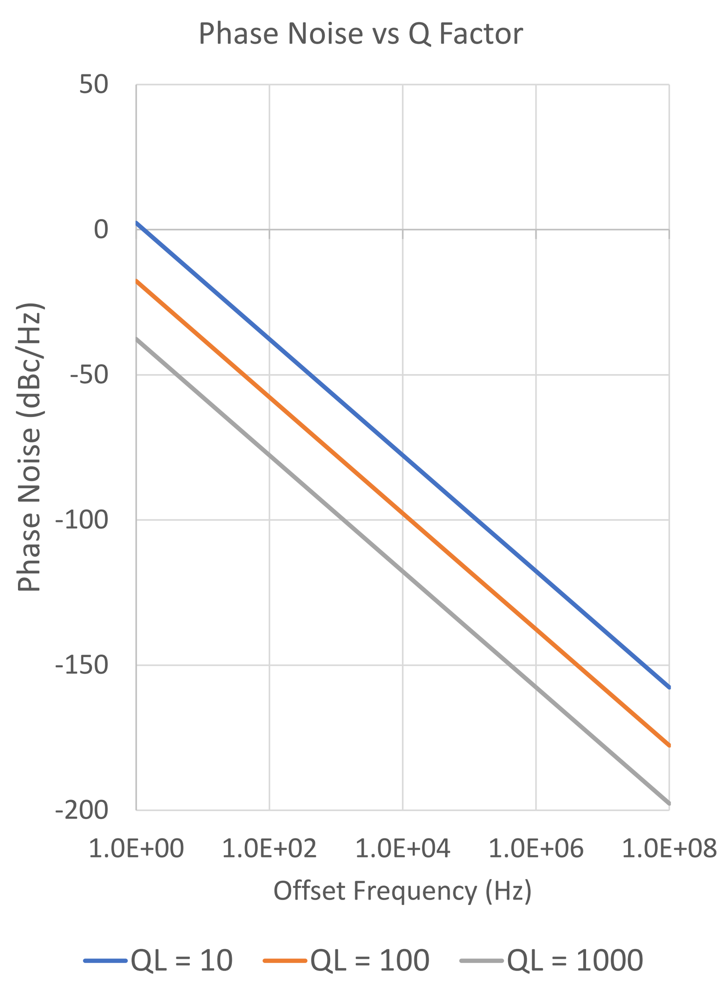
T : Absolute Temperature

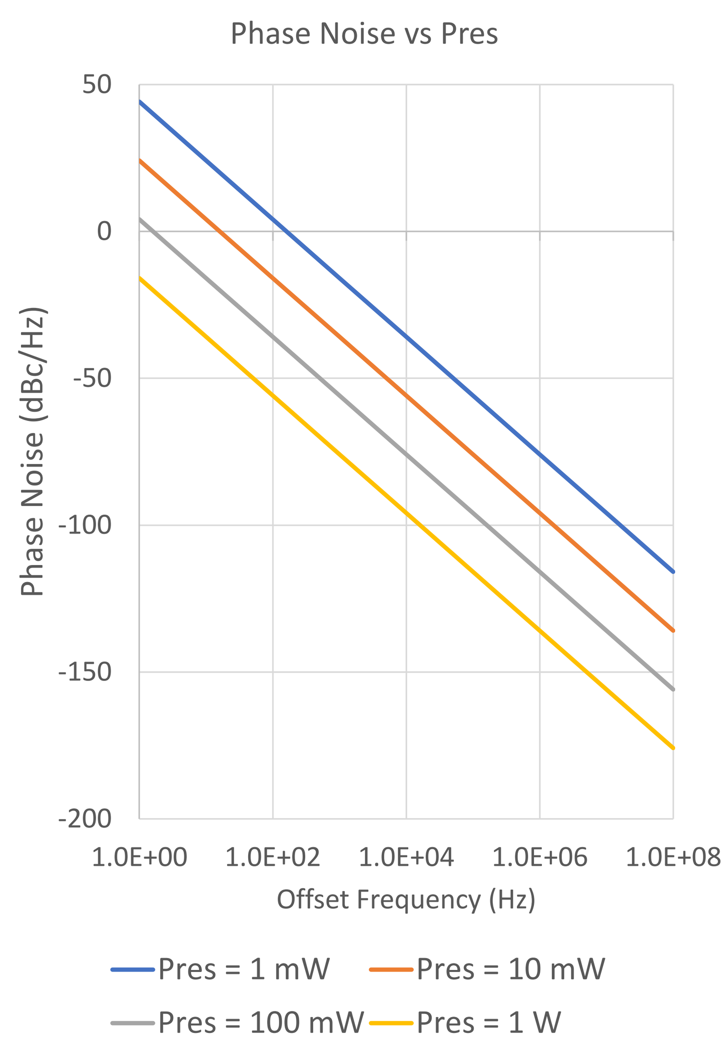
F : Excess Noise Number

k : Boltzmann Constant

Q_L: Loaded quality-factor of the Resonator

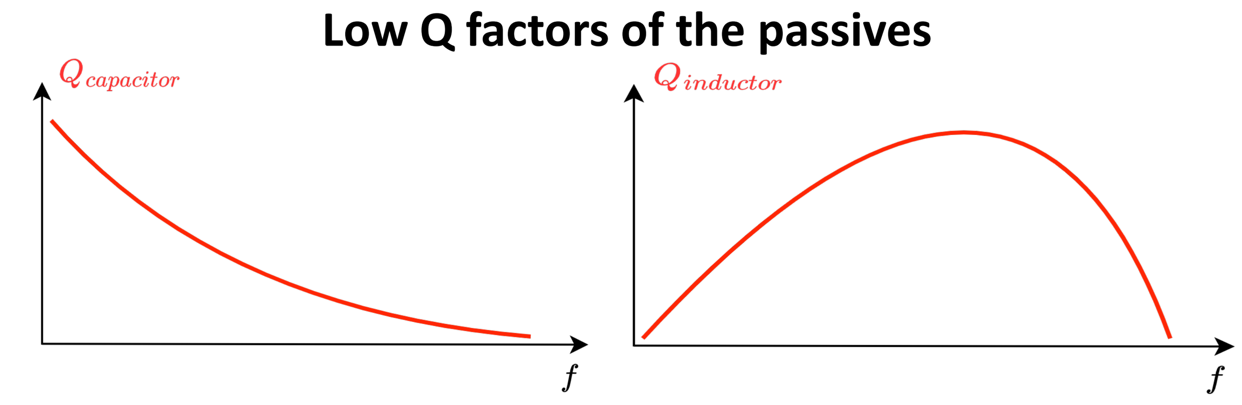
P_{res}: Power Dissipated at the Resonator



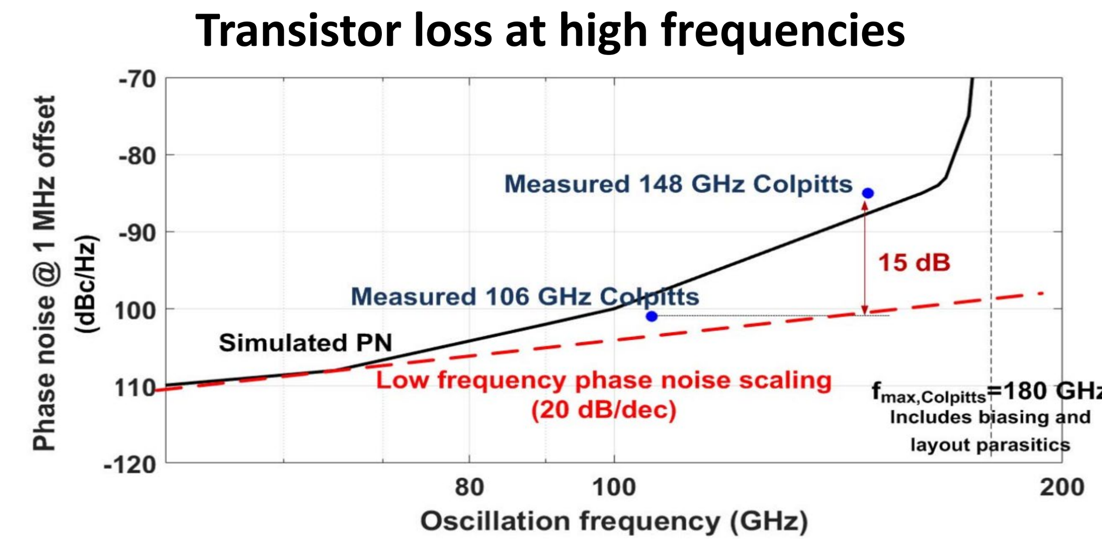


Challenges

Low Q factors of the passives

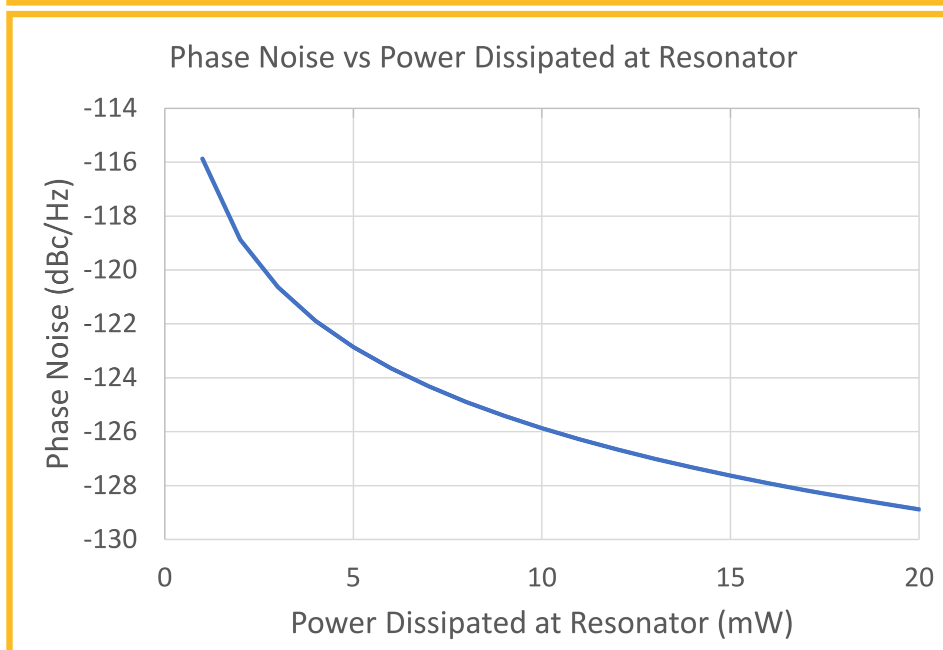


Transistor loss at high frequencies

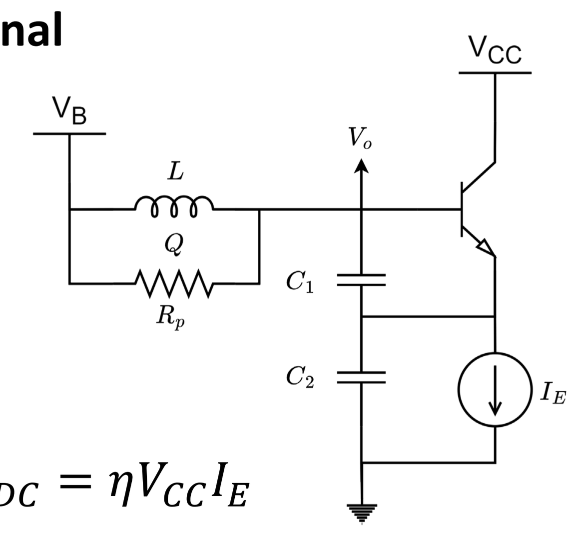


A. Imani and H. Hashemi, "Frequency and Power Scaling in mm-Wave Colpitts Oscillators," in IEEE Journal of Solid-State Circuits, vol. 53, no. 5, pp. 1338-1347, May 2018.

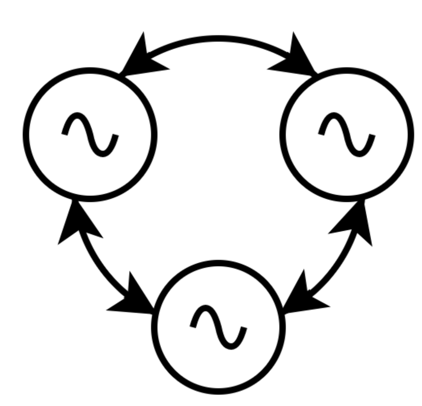
Improving Phase Noise by Increasing Power



Conventional



$$P_{res} = \eta P_{DC} = \eta V_{CC} I_E$$



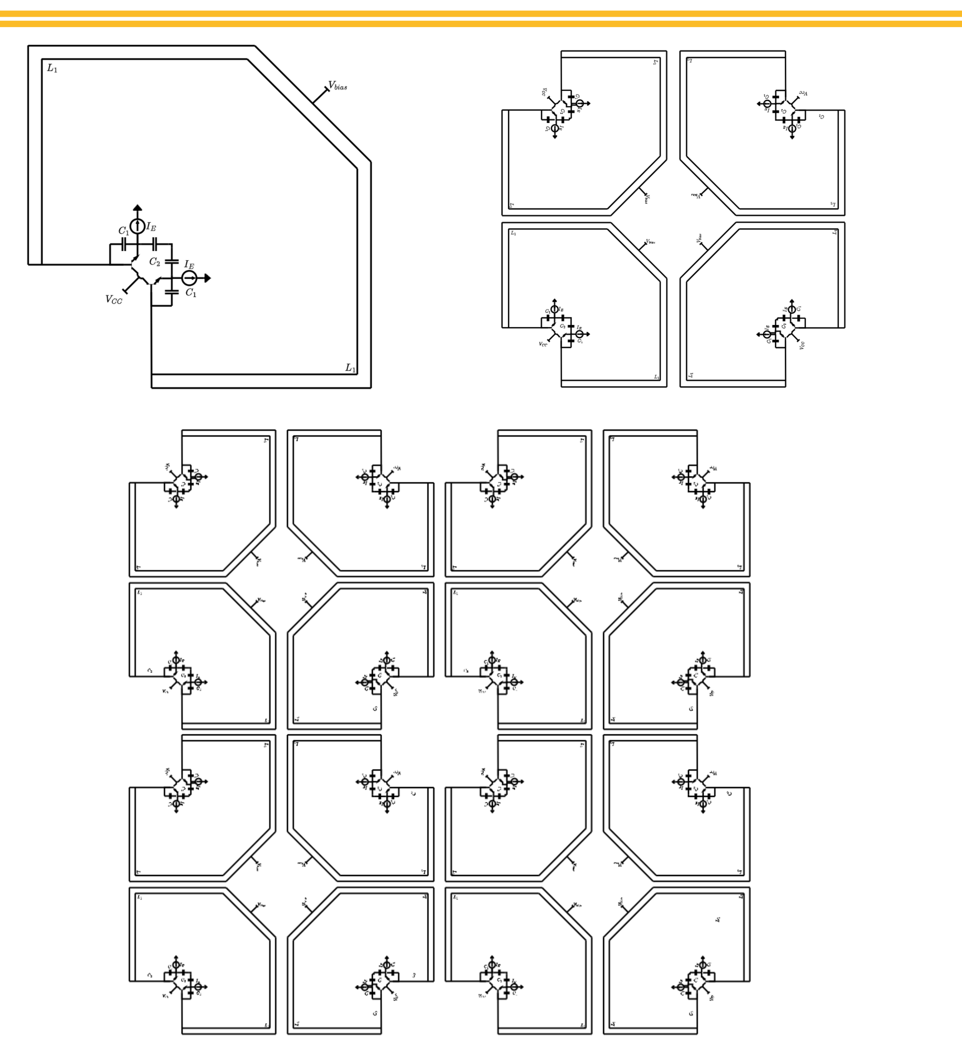
Coupled Oscillators

$$f_{osc}\Big|_{system} = \frac{1}{N}\sum_{i=1}^{N} f_{osc,i}$$

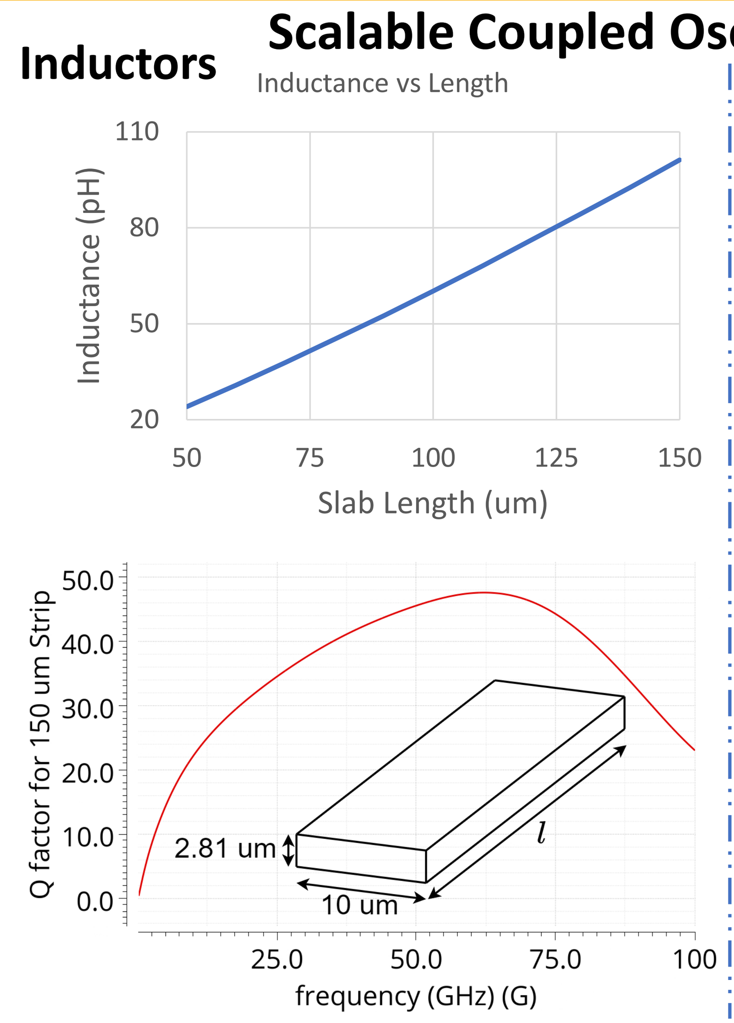
$$P\Big|_{system} = N\,P_{single}$$

$$\mathcal{L}(\Delta f)\Big|_{system} = \frac{1}{N}\mathcal{L}(\Delta f)\Big|_{single}$$

Scalable Coupled Oscillator Design

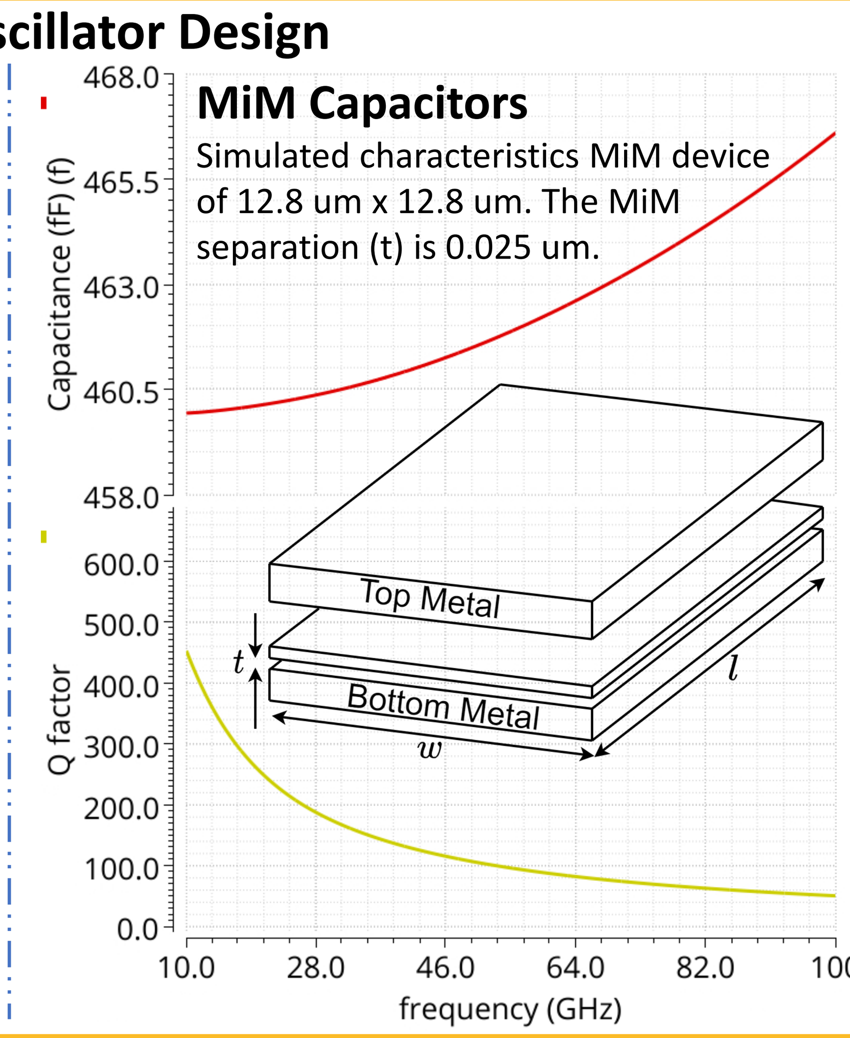


Inductors



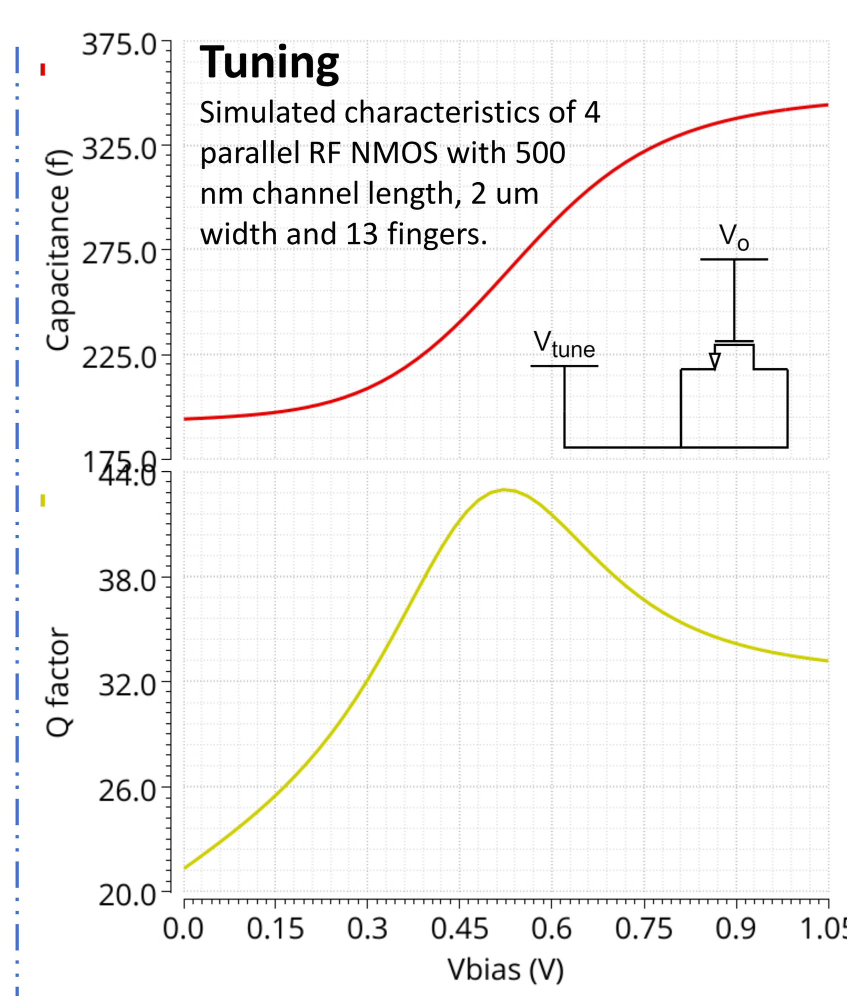
MiM Capacitors

Simulated characteristics MiM device of 12.8 um x 12.8 um. The MiM separation (t) is 0.025 um.



Tuning

Simulated characteristics of 4 parallel RF NMOS with 500 nm channel length, 2 um width and 13 fingers.



Implementation and Results

Design/ Author		VCC (V)	Current	Phase Noise*	Max. Frequency	Tuning Range	FoM_1 *	FoM_T *	No of Cores	Technology
Zhan ISSCC 2023		0.5 V	50 mA	-115.3 dBc/Hz	25.8 GHz	4.4 GHz (18.2 %)	-190.6 dB	-195.8 dB	4	65 nm CMOS
Shu ISSCC 2023		12 mW		-115.6 dBc/Hz	28 GHz	4.9 GHz (17.5 %)	-193.3 dB	-198.2 dB	4	40 nm CMOS
Peng ISSCC 2022		1.35 V	2.6 mA	-112.0 dBc/Hz	17 GHz	3.6 GHz (23.7 %)	-189.9 dB	-197.4 dB	2	130 nm SiGe
Jia ISSCC 2022		0.65 V	192 mA	-111.7 dBc/Hz	60.2 GHz	6.6 GHz (10.9 %)	-185.7 dB	-186.4 dB	16	65 nm CMOS
Jia ISSCC 2021		0.4 V	15.3 mA	-101.4 dBc/Hz	60.4 GHz	8 GHz (14.2 %)	-182.2 dB	-185.2 dB	16	65 nm CMOS
This Work	Design 1	1.5 V	5.5 mA (max)	-101 dBc/Hz	37 GHz	4.25 GHz (12 %)	-184.5 dB	-186.2 dB	1	180 nm SiGe
	Design 2	1.5 V	22 mA (max)	-109 dBc/Hz	34 GHz	3.92 GHz (11 %)	-188.2 dB	-189.9 dB	4	180 nm SiGe
	Design 3	1.5 V	88 mA (max)	-115 dBc/Hz	32 GHz	3.80 GHz (11 %)	-188.2 dB	-190.0 dB	16	180 nm SiGe
	Design 4	1.5 V	352 mA (max)	-121 dBc/Hz	32 GHz	3.80 GHz (11 %)	-188.2 dB	-190.0 dB	64	180 nm SiGe
	Design 5	1.5 V	1408 mA (max)	-127 dBc/Hz	32 GHz	3.80 GHz (11 %)	-188.2 dB	-190.0 dB	256	180 nm SiGe

$$FoM_1 = PN\Big|_{dB} - 20\log\left(\frac{f}{\Delta f}\right) + 10\log\left(\frac{P_{DC}}{1mW}\right)$$

$$FoM_T = PN\Big|_{dB} - 20\log\left(\left(\frac{f_{osc}}{\Delta f}\right) * \left(\frac{TR\%}{10}\right)\right) + 10\log\left(\frac{P_{DC}}{1\text{ mW}}\right)$$

* Phase noise, FoM, FoM_T and are considered with 1 MHz offset from carrier frequency.

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Clearance Number: CL#00-0000
Poster Number: RPC#

Significance/Benefits to JPL and NASA: The long-term goal of this collaboration is to develop a compact W-band transceiver for application in radars in upcoming missions. The development of this compact radar has several significant building blocks that require innovations in mm-wave circuit design and development to produce a compact system. One of which is a very low phase noise oscillator that results in a high-performance LO for RF and a high-performance clock for digital subsystems of the radar. Hence resulting in high performance radar that allows optimization of velocity and range ambiguities for radar landers and precise measurements in minuscule fragments of molecules and particles of space and earth atmospheric environment.

Publications:
NA

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